APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,104	06/15/2005	Otto Steinbusch	US02 0610 US2	9255

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EXAMINER
MERANT, GUERRIER

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
12/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/539,104	STEINBUSCH, OTTO
	Examiner	**Art Unit**	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2007*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☒ All   b)☐ Some *   c)☐ None of:

  1.☐ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
  Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   In view of the Appeal Brief filed on 5/11/2007, PROSECUTION IS HEREBY

REOPENED. The new grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the

following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply

under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed

by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and

appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth

in 37 CFR 41.20 have been increased since they were previously paid, then appellant

must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by

signing below:

Jacques Louis Jacques.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Casseti et al. (US 6,311,302 B1) and further in view of **Nadeau-Dostie et al (US**

2002/0184562 A1).

Claim 1: **Casseti et al** substantially a method of coupling a plurality of test access port

(TAP) controllers to a single external interface *(col. 3, lines 6-19, see fig. 1)*,

comprising: resetting a first bit in each of plurality of chip-level TLM controllers *(col.6,*

lines 1-10) a known state *(on/off or 0 or 1)*; producing a first signal based, at least in

part, on the state of the first bit in each of the plurality of TLM controllers *(depending*

upon the command loaded into the internal TLM register, the TLM module enables or

disables various TAPs in a system by controlling TMS- col. 2, lines 21-50); selecting

one of the plurality of TLM controllers based, at least in part, on the first signal *(this*

functionality is done by the Chip-level TML 40- see figs.1 or 2); coupling an external

input terminal to an input terminal of the selected one of the plurality of TLM controllers;

and coupling an output terminal of the selected one of the plurality of TLM controllers to

an external output terminal *(col.4, lines 53-65)*. But, **Cassetti et al** fails to explicitly

teach that a TAP could also replace the TLM controller. However, **Nadeau-Dostie et al**

teaches a method of coupling a plurality of test access port (TAP) controllers to a

single external interface comprising: resetting a first bit in each of plurality of TAP

controllers a known state *(on/off or 0 or 1)*, producing a first signal based, at least in

part, on the state of the first bit in each of the plurality of TAP controllers and selecting

one of the plurality of TLM controllers based, at least in part, on the first signal *(e.g.*

[0010], [0031] and [0034]). Therefore, at the time the invention was made, it would

have been obvious to a person of ordinary skill in the art to implement the method of

Cassetti et al with method taught by **Nadeau-Dostie et al** in order "to *provide a novel,*

multiple TAP circuit architecture and a method of designing a circuit containing a

plurality of TAPs which is compliant with the standard, which does not require

modification of any of the embedded TAPs and which can be structurally tested, any

which can effectively control any or all of the TAPs without the need for non-standard

Signals (e.g. [0007], Nadeau-Dostie et al).

Claim 2: **Casseti et al.** and **Nadeau-Dostie et al** teach a method as in claim 1 above,

wherein the TAP controller comprises a finite state machine and a plurality of registers

(col. 5, lines 7-28- Cassetti et al).

Claims 3 and 4: **Casseti et al.** and **Nadeau-Dostie et al** teach a method as in claim 2

above, further comprising toggling *(inverting)* the first bit in the selected one of the

plurality of TAP controllers; and repeating steps (b) through (e) *(col. 5, lines 56-67 & col.*

6, lines 1-10- Cassetti et al).

Claims 5 and 6: **Casseti et al.** and **Nadeau-Dostie et al** teach a method as in claim 3

above, wherein the plurality of TAP controllers are disposed on a single integrated

circuit and the first signal is produced within the single integrated circuit *(see figs. 1 & 2*

for connection- col. 4, lines 53-68 & col. 5, lines 1-6- Cassetti et al).

Claim 7: **Casseti et al.** and **Nadeau-Dostie et al** teach a method as in claim 6 above,

further comprising receiving from a source external to the single integrated circuit, a

clock signal *(see figs 1& 2 wherein externals signals TCK, TMS, TDI, TRST are being*

received by the integrated circuit 10- Cassetti et al).

Claims 8-10, 12 and 13: **Casseti et al.** substantially teaches an integrated circuit *(item*

10, Figs. 1 & 2), comprising: a plurality of functional blocks *(items 12 & 14, Figs. 1 & 2)*,

each functional block having a test access port (TAP), and TML controller coupled

thereto *(items 16, 18, 30, 32- Figs. 1 & 2)*; each TLM controller including a first register

bit *(items 20,22 & 36,34- Figs. 1 & 2)*, each first register bit adapted to produce a

known output state in response to a reset signal *(depending upon the command*

loaded into the internal TLM register which is resetting after each instruction, *the TLM*

module enables or disables various TAPs in a system by controlling TMS- col. 2,

lines21-50 & col. 6, lines 1-10), each first register bit further adapted to toggle in

response to a register write operation; and routing logic *(CTLM, item 40; fig. 1&2)*

adapted to selectively provide, based at least in part on the state of the plurality of first

register bits, a communication path between an external input signal source and an

input terminal of a selected one of the TLM controllers *(col. 5, lines 56-67 & col. 6, lines 1-10, see Figs. 1&2)*. But, **Cassetti et al** fails to explicitly teach that a TAP could also replace the TLM controller. However, **Nadeau-Dostie et al** teaches an integrated circuit *(e.g. fig. 1)*, comprising: a plurality of functional blocks *(items 24, 22 and 20, fig. 1)*, each functional block having a test access port (TAP, e.g. items 14, 16 and 12, fig. 1) controller coupled thereto wherein each TAP is coupled to a first register incorporated in the Master TAP for resetting a first bit in each of plurality of TAP controllers a known state *(on/off or 0 or 1)*, producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers and selecting one of the plurality of TLM controllers based, at least in part, on the first signal *(e.g. [0010], [0031] and [0034])*. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to implement the circuit of **Cassetti et al** with circuit taught by **Nadeau-Dostie et al** in order "to *provide a novel, multiple TAP circuit architecture and a method of designing a circuit containing a plurality of TAPs which is compliant with the standard, which does not require modification of any of the embedded TAPs and which can be structurally tested, any which can effectively control any or all of the TAPs without the need for non-standard Signals (e.g. [0007], Nadeau-Dostie et al)*.

Claim 11: **Casseti et al.** and **Nadeau-Dostie et al** teach an integrated circuit as in claim 9 above, wherein a transition between the selectively provided communication paths is transparent to an external observer *(col. 4, lines 53-66- once an instruction is loaded,*

the TLM 40 selects which Tap to access without the help of user or observer- Cassetti et al).

Claim 14: **Casseti et al.** and **Nadeau-Dostie et al** teach an integrated circuit as in claim 13 above, wherein the each of the plurality of TAP controllers has a second input terminal adapted to receive a clock signal *(TCK, fig. 1)*, a third input terminal adapted to receive mode select signal (*TMS, fig.1)*, and a fourth input terminal adapted to receive a reset signal *(TRST, fig.1)*; wherein the plurality of second input terminals are coupled in common, the plurality of third input terminals are coupled in common, and the plurality of fourth input terminals are coupled in common *(col. 5, lines 7-28- Cassetti et al)*.

Claim 15: **Casseti et al.** and **Nadeau-Dostie et al** teach an integrated circuit of claim 14 above, further comprising a chain bit *(item 22 figs. 1& 2- Cassetti et al)* disposed in a first one of the plurality of TAP controllers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.
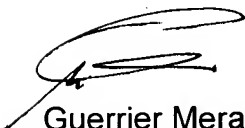
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or
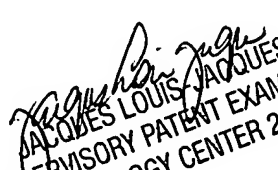
Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Guerrier Merant
11/28/07